ARRAY SUBSTRATE, METHOD FOR MANUFACTURING THE SAME, AND DISPLAY DEVICE

This application is a 371 of PCT/CN2013/086741 filed on Nov. 8, 2013, which claims priority benefits from Chinese Patent Application Number 201310222271.7 filed Jun. 5, 2013, the disclosure of which is incorporated herein by reference.

TECHNICAL FIELD

The present invention relates to the field of display technology, and particularly, to an array substrate, a method for manufacturing the same, and a display device.

BACKGROUND ART

Liquid crystal display made of thin film transistors has characteristics such as small size, low power consumption, no radiation, and so on, thus dominates the current flat panel display market. Liquid crystal panel is an important component of the liquid crystal display, and comprises an array substrate, a color filter substrate, and a liquid crystal layer filled between the array substrate and the color filter substrate.

The array substrate comprises a plurality of thin film transistors arranged in an array, which are formed on a glass or plastic substrate by sputtering chemical vapor deposition and other processes. The gate electrodes of the thin film transistors in the same row are connected together by a gate line, and the source electrodes of the thin film transistors in the same column are connected together by a data line, wherein the materials of the gate line and the data line are typically tantalum, chromium, molybdenum, or an alloy of at least two of them.

With the gradually increasing size of the liquid crystal display, the lengths of the gate line and the data line in the array substrate also increase, resulting in increasing resistance of the gate line and the data line. Since the signal delay time of a signal line is proportional to the resistance of the signal line, an increase in the resistance of a signal line will result in an increase in the signal delay time of the signal line. When the signal delay time reaches to a certain extent, some pixels are not fully charged, resulting in uneven brightness and lower contrast of the liquid crystal display, thereby the quality of the image displayed on the liquid crystal display is seriously affected.

SUMMARY

The present invention provides an array substrate, a method for manufacturing the same, and a display device, which solve the problem that the large resistance of the long gate line and the long date line in a large-size liquid crystal display will lead to a decline in the image display quality of the liquid crystal display.

To achieve the above object, the present invention employs the following technical solutions.

The present invention provides a method for manufacturing an array substrate, comprising:

(1) sequentially forming a first adhesion enhancement layer, a first copper-bearing metal layer and a photoresist layer on a substrate, and respectively forming a reserved region and a removal region by performing exposure and development on the photoresist layer using a mask plate, wherein the reserved region corresponds to a pattern forming region; simultaneously processing the first adhesion enhancement layer, the first copper-bearing metal layer and the photoresist layer in the removal region by a single wet etching process, to form a first adhesion enhancement intermediate layer corresponding to the first adhesion enhancement layer, a first copper-bearing metal intermediate layer corresponding to the first copper-bearing metal layer and the photoresist layer thereon in the reserved region; and simultaneously processing the first adhesion enhancement intermediate layer, the first copper-bearing metal intermediate layer and the photoresist layer thereon by a dry etching process, then stripping off the photoresist layer, to form a patterned first adhesion enhancement layer and a patterned first copper-bearing metal layer respectively, wherein the first adhesion enhancement layer is a metal layer for enhancing adhesion of the first copper-bearing metal layer to the substrate.

The patterned first copper-bearing metal layer may be a pattern comprising gate electrodes.

The pattern comprising gate electrodes comprises gate electrodes and a gate lines formed in the same layer.

The patterned first copper-bearing meal layer may be a pattern comprising source electrodes and drain electrodes.

The pattern comprising source electrodes and drain electrodes comprises source electrodes, drain electrodes and data lines formed in the same layer.

The material of the first copper-bearing metal layer is copper or copper alloy.

The material of the first adhesion enhancement layer is any one of tungsten, tantalum, titanium, molybdenum, molybdenum alloy and titanium alloy.

The thickness of the first adhesion enhancement layer is 100~1000 Å, and the thickness of the first capper-bearing metal layer is 1500~5000 Å.

After the single wet etching process, the width of the formed first adhesion enhancement intermediate layer is larger than the width of the formed first copper-bearing metal intermediate layer, so that the first adhesion enhancement intermediate layer forms a step structure with respect to the first copper-bearing metal intermediate layer, and the step structure will be removed by a subsequent dry etching process.

The above method for manufacturing an array substrate further comprises: (2) sequentially forming a gate insulation material layer and a semiconductor material layer on the substrate subjected to step (1), and processing the semiconductor material layer by a patterning process to form a pattern comprising an active layer, wherein the gate insulation material layer is used for forming a gate insulation layer; and (3) sequentially forming a second adhesion enhancement layer, a second copper-bearing metal layer and a photoresist layer on the substrate subjected to step (2), and respectively forming a reserved region and a removal region by performing exposure and development on the photoresist layer using a mask plate, wherein the reserved region corresponds to a pattern forming region; simultaneously processing the second adhesion enhancement layer, the second copper-bearing metal layer and the photoresist layer in the removal region by a wet etching process, to form a second adhesion enhancement intermediate layer corresponding to the second adhesion enhancement layer, a second copper-bearing metal intermediate layer corresponding to the second copper-bearing metal layer and the photoresist layer thereon in the reserved region; and simultaneously processing the second adhesion enhancement intermediate layer, the second copper-bearing metal intermediate layer and the photoresist layer thereon by a dry